Design, Fabrication, and Characterization of Dense Compressible Microinterconnects

Paul K. Jo, *Student Member, IEEE*, Muneeb Zia, *Student Member, IEEE*, Joe L. Gonzalez, *Student Member, IEEE*, Hanju Oh, *Student Member, IEEE*, and Muhannad S. Bakir, *Senior Member, IEEE*

***Abstract*— This paper presents gold passivated NiW compressible microinterconnects (CMIs) with 75 μm height and 150 μm in-line pitch. The CMIs are batch fabricated using CMOS-compatible processes. The fabricated CMIs have a measured compliance of up to 13.12 mm/N and demonstrate 45 μm elastic vertical range of motion. Moreover, the CMIs are shown to return to their original geometrical profile after several deflections and consequently are able to maintain contact with their corresponding pads at all times. The measured four-point resistance of a CMI, which includes contact resistance, is as low as 176.3 mΩ.**

***Index Terms*— 3-D IC, interconnect, microelectromechanical system (MEMS), microspring, multichips, packaging, probe tip, temporary interconnection.**

I. Introduction

INTERCONNECTS play a critical role in virtually all microelectronic applications including digital, mixed-signal, photonic, microelectromechanical systems (MEMS), and sensor microsystems [1], [2]. They are key in influencing microsystem form factor, electrical performance, power consumption, signal integrity, and a host of other system metrics. Of particular importance are first-level interconnects, which are used to electrically interconnect and mechanically bond a die to a package substrate. The density, electrical attributes, and mechanical properties of first-level interconnects impact the overall mechanical integrity of the resulting assembled microsystem, signaling bandwidth density between dice, and power supply noise in digital microsystems. While solder bumps have become a key technology for first-level interconnects, the technology unfortunately leaves a number of attributes desired in modern microsystems. First, solder bump density scaling is difficult particularly due to solder shorting, increased height uniformity constraints (on the substrate and the bumps) for robust assembly, and reduced mechanical strength of the resulting bonds. This is particularly a challenge when one needs to form bumps with multiple densities on the same chip, as is required in the embedded multidie interconnect bridge technology [3] and other emerging heterogeneous interconnection platforms. When solder shorting occurs, it is virtually impossible to undo, and it is often the case that the whole package or module has to be disposed of, which is a costly solution. Additionally, underfill is usually required for solder bump assembled dice. Die rework or replacement is difficult and costly, particularly for fine-pitch applications.

Compliant first-level interconnects, which can provide electrical interconnections between tiers through a pressure contact mechanism, can circumvent many of the challenges in solder bumps as no reflow processes are needed, no metallurgical bonds are formed, no underfill is required, and any mechanical compression on the interconnects does not cause lateral spreading, which might result in shorting. These benefits have spurred much research in compliant interconnects [4]–[16], which will be discussed later. There are many commercial applications for mechanically compliant interconnects as second-level interconnects as well. One relevant application space relates to socketed systems, as in Intel's Core i7 and AMD's Opteron processors land grid array (LGA) sockets; since the LGA socket interconnections are pressure-contact-based, they allow for a simple replacement or upgrade of the interconnected processor. Moreover, compliant interconnects have been used in the assembly of interposers and probe cards for wafer sorting and other testing applications.

A number of free-standing compliant interconnect technologies have been presented in the literature as first-level interconnects, including sea-of-leads (SoLs) [4]–[6], G-Helix [7], Flex-Connect [8], β-Helix [9], compliant die-package interconnects [10], and mechanically flexible interconnects [11]–[13]. Additional compliant interconnects include rematable spring interconnects [14], J-springs [15], and coiled microsprings [16], which are upward-curved interconnects. To better differentiate some of the compliant interconnect technologies, a comparison is summarized in Table I. Although many compliant interconnect technologies exist, several significant issues limit their utilization in emerging microsystems. For example, while the demonstrated lithographically defined compliant interconnects are based on simple fabrication processes, their compliance and elastic range are limited [7], [9]. Moreover, while other compliant interconnects, which are fabricated by stress engineering, have demonstrated a relatively large elastic range of motion and a high

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P. K. Jo, M. Zia, J. L. Gonzalez, and H. Oh are with the Electrical and Computer Engineering Department, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: paul.jo@gatech.edu).

M. S. Bakir is with the School of Electrical and Computer Engineering, Georgia Technology, Atlanta, GA 30332 USA (e-mail: mbakir@ece.gatech.edu).

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TABLE I
COMPARISON OF COMPLIANT INTERCONNECTS

Technology	Pitch (μm)	Height (μm)	Compliance (out-of-plane) (mm /N)	Vertical range of motion (μm)
Sea-of-leads (SoL) [4]	> 120	60 – 90	0.5 – 2	< 30
G-Helix [7]	100	78	14.7	NA
β-Helix [9]	200	110	> 7.1	NA
Rematable spring interconnects [14]	180	50	218	32
J-Springs [15]	> 30	100	> 3500	NA

compliance, there is poor control over their final geometric design, and they possess very high compliance, which is not desirable [14], [15].

To this end, this paper presents highly flexible and elastically deformable interconnects, which we call compressible microinterconnects (CMIs). The key features of the CMI technology include: 1) lithographically defined, CMOS-compatible, and simple fabrication; 2) large elastic range of motion to compensate for surface nonuniformity on the attaching substrate, especially for a large die or interposer assembly, and CTE mismatch induced warpage; 3) high degree of freedom in interconnect design; 4) pressure-based and non-permanent contact mechanism; since CMIs can provide temporary interconnections, they can enable chips, interposers, or packages to be replaced, hence increasing system yield; and 5) since a thermocompression process is not required, the assembly process is simplified as bonding parameters such as temperature need not be considered [17]. With the aforementioned key features, the CMI technology can be a key enabler for the seamless integration of heterogeneous systems while offering design versatility and replaceability for next-generation microelectronic applications, as illustrated in Fig. 1.

In addition to the aforementioned application, CMIs can be used as follows: 1) Since CMIs can be easily engineered to have either low or high contact forces, they are well-suited for microprobe tips; a microprobe tip should be neither too stiff as to inflict damage on a pad nor too flexible so that it cannot scratch through a formed oxidized layer. Therefore, a balanced contact force is necessary during probing the device under test. 2) These temporary interconnections can also enable the reuse of CMOS biosensors for cell-based assays by disposing of an integrated replaceable interface that sits atop the biosensor rather than the biosensor itself [18]. This reuse potentially reduces the cost of operation for biosensors, which are often irreversibly contaminated by blood or other cellular tissue [19], [20].

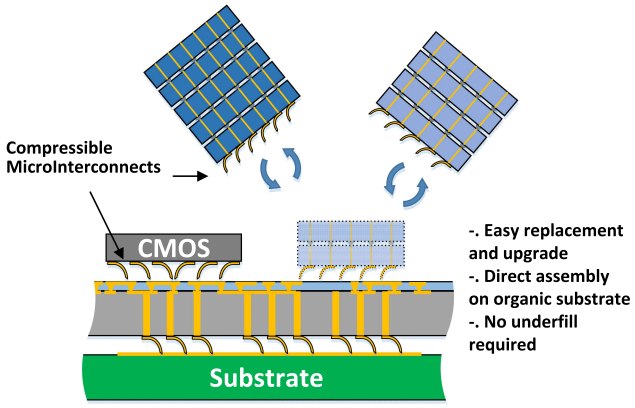


Fig. 1. Multichip integrated system with CMIs.

This paper is organized as follows. Section II describes the CMI design with the goal of maximizing its mechanical elastic deflection. Section III reports the CMOS-compatible fabrication process. Section IV describes the mechanical and electrical properties of the CMIs. Finally, Section V is the conclusion.

II. DESIGN OF CMIs

Since CMIs are lithographically defined and agnostic to substrate material (compatible with glass, ceramic, FR4, etc.), many different interconnect designs can be explored. For example, the tips of the CMIs can be designed such that the contact region between the CMI tip and the corresponding contact pad is controlled. The sizes and shapes of these contact regions can be adjusted via the CMI tip. For example, a CMI that is designed to have a platform-like tip, as shown in Fig. 2(a), may form a large contact area onto the mating pad; the CMI in this example possesses 80 μm of vertical height (h_{CMI}) and 190 μm of length (ℓ_{CMI}) from the junction of the anchor to the tip. Alternatively, a CMI with a "blunt" tip is shown in Fig. 2(b), which forms a line contact with

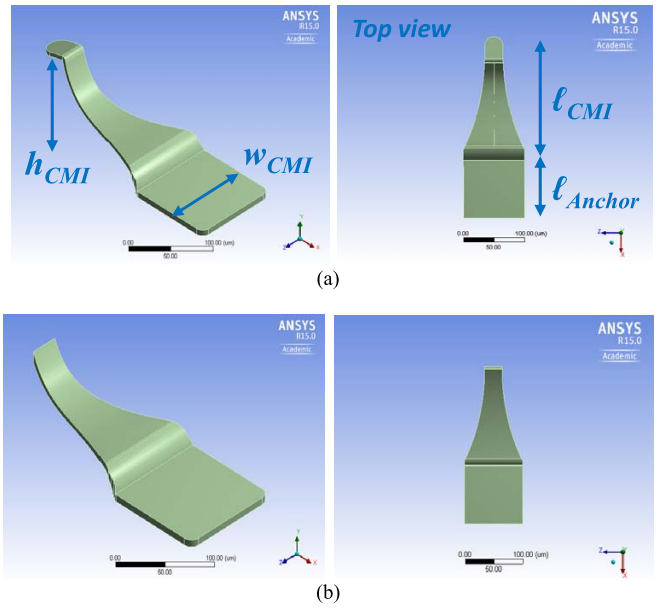


Fig. 2. ANSYS FEM simulation geometry of the CMI with (a) platform-like tip and (b) blunt tip.

TABLE II
SPECIFICATIONS OF CMIs

	h_{CMI}	ℓ_{CMI}	ℓ_{Anchor}	w_{CMI}
CMI for large area contact	80 μm	190 μm	100 μm	100 μm
CMI for single line contact	75 μm	150 μm	100 μm	100 μm

the mating pad. The shown CMI is approximately 75 μm in height (h_{CMI}) and 150 μm in length (ℓ_{CMI}). Both CMI designs have a square anchor of 100 μm length (ℓ_{Anchor}) and 100 μm width (w_{CMI}). The geometric specifications of the CMIs are summarized in Table II.

In order to maximize the vertical elastic range of motion, CMIs with an approximately tapered design are implemented in an effort to uniformly distribute stress during deflection [11]. In addition, CMIs are fabricated using NiW to enhance this mechanical advantage and to be more durable under stress (relative to copper) [21]. Specifically, NiW can achieve a yield strength of 1.93 GPa, whereas Cu has a yield strength of 136 MPa [22]. Therefore, compared to Cu, NiW enables the CMI to withstand higher stress before experiencing plastic deformation, which would cause permanent change to the geometric profile of the CMI and thus may exacerbate interconnect reliability. Even though Cu has better electrical characteristics than those of NiW, it is the mechanical performance of the compliant interconnect that we wish to exploit, hence NiW has been used; electroless gold plating is used to passivate the CMI to prevent oxidation, which helps to lower contact resistance [12]. The CMI has a vertically upward-curved geometry, and this ensures that the contact region formed during deflection remains on the tip of the CMI. To date, stress engineering has been employed to fabricate such upward-curved interconnects [14]–[16], which

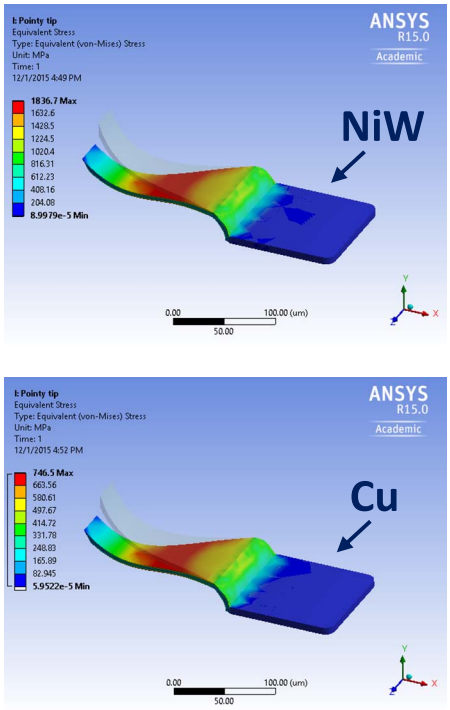


Fig. 3. ANSYS FEM indentation simulation of the CMI with NiW (top) and Cu (bottom).

limits their application space significantly due to its limited control in obtaining targeted geometric specifications, which may be problematic when undergoing batch fabrication. Moreover, difficulty in achieving targeted geometric specifications contributes to difficulty in achieving certain mechanical (and electrical) characteristics such as a specified compliance. However, this paper, for the first time, demonstrates the fabrication of upward-curved compliant interconnects utilizing a lithographic process, which is not only simpler but allows for more versatility in design (more geometries, materials, etc.) relative to stress engineering, as will be shown in Section III.

The CMI was modeled using ANSYS finite-element method (FEM), as shown in Fig. 3. Both Cu- and NiW-based CMIs were deformed to a vertical depth of 45 μm in the simulations. The results of the simulations show that the maximum von Mises stress for the NiW CMI is approximately 1.83 GPa under 45 μm vertical deformation, which is less than the assumed yield strength of NiW (1.93 GPa). However, the maximum von Mises stress for the Cu CMI is approximately 746 MPa, which is larger than the yield strength of Cu (136 MPa), and hence plastic deformation is experienced by the Cu CMI (only linear model used; plastic deformation omitted in model). Thus, the mechanical characteristics of the NiW CMI ensure that the CMI does not undergo permanent plastic deformation and can return to its original position despite its large vertical deflection, which is 60% of its total height in this case (which is not a limit).

III. FABRICATION PROCESS

The fabrication process of CMIs is illustrated in Fig. 4. The first step is the spin coating of a sacrificial photoresist layer onto the surface of the wafer followed by patterning

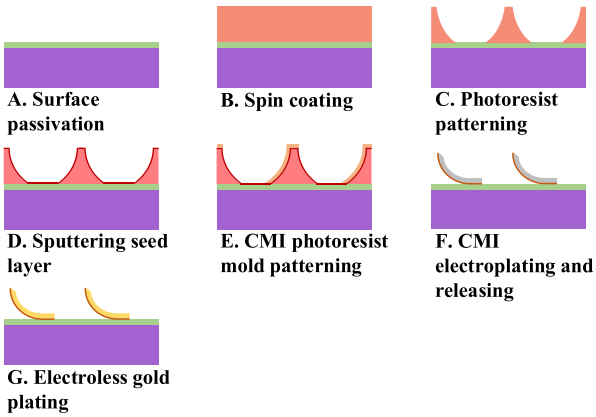


Fig. 4. Fabrication process of CMIs. (A) Surface passivation. (B) Spin coating. (C) Photoresist patterning. (D) Sputtering seed layer. (E) CMI photoresist mold patterning. (F) CMI electroplating and releasing. (G) Electroless gold plating.

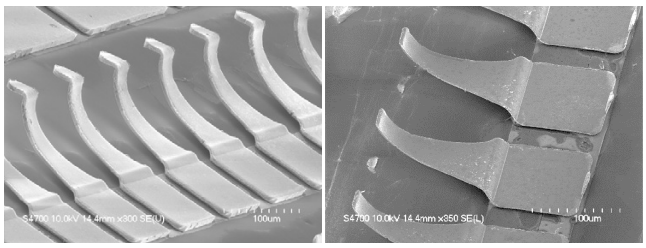


Fig. 5. SEM image of the CMIs with the platform-like tip (left) and blunt tip (right).

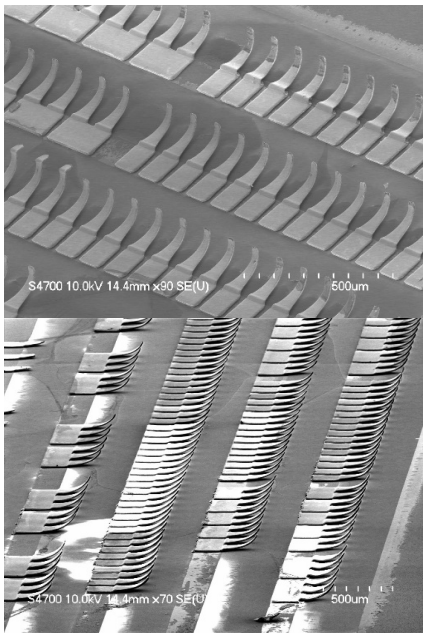


Fig. 6. SEM images of a CMI array.

the sacrificial photoresist to exhibit a curved sidewall profile. Next, a Ti/Cu/Ti seed layer is deposited followed by a photoresist film to form the electroplating mold. During electroplating, NiW is deposited within the mold to form the CMIs. After electroplating, the mold photoresist layer, the Ti/Cu/Ti seed layer, and the sacrificial photoresist layer

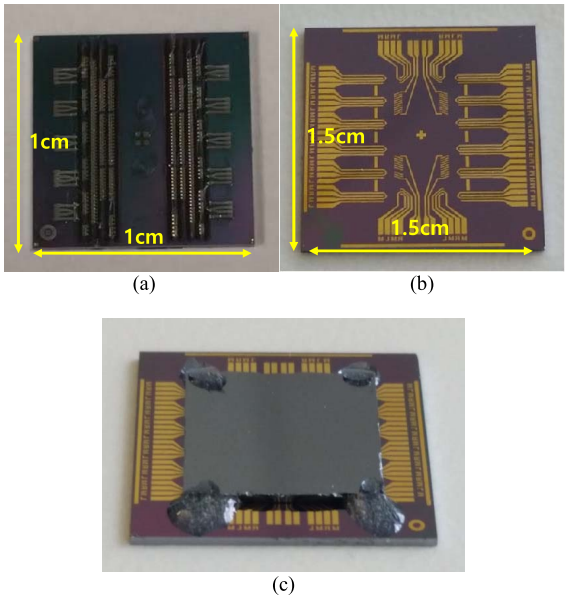


Fig. 7. (a) 336 CMIs were batch fabricated on a chip and (b) then flip-chip bonded to the test substrate. (c) Chip was bonded by applying epoxy.

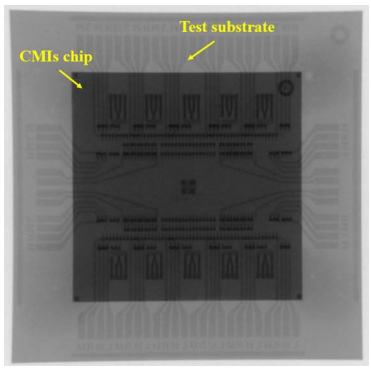


Fig. 8. X-ray image of the assembled chip.

are removed in sequence leaving behind free-standing CMIs. Finally, the CMIs are passivated by electroless gold plating in order to prevent the oxidation of NiW, which negatively affects mechanical and electrical characteristics. CMIs are immersed in gold electroless plating solution such that all exposed surfaces of the CMIs are coated with gold [12]. In order to investigate the differences in mechanical and electrical properties as a function of thickness, two samples of different thicknesses (7.6 and 10.5 μm) are fabricated. Figs. 5 and 6 show SEM images of the fabricated CMIs.

IV. Results and Discussion

A. Flip-Chip Bonding

A chip containing 336 CMIs was batch-fabricated [Fig. 7(a)] and flip-chip bonded onto a silicon substrate containing gold pads on its surface for four-point resistance measurements [Fig. 7(b)]. Ti/Cu/Au were deposited using an evaporator with thicknesses of 50/300/10 nm, respectively, in order to make the pads. After aligning and lowering the chip into contact with the substrate, epoxy was applied to each of the four chip corners

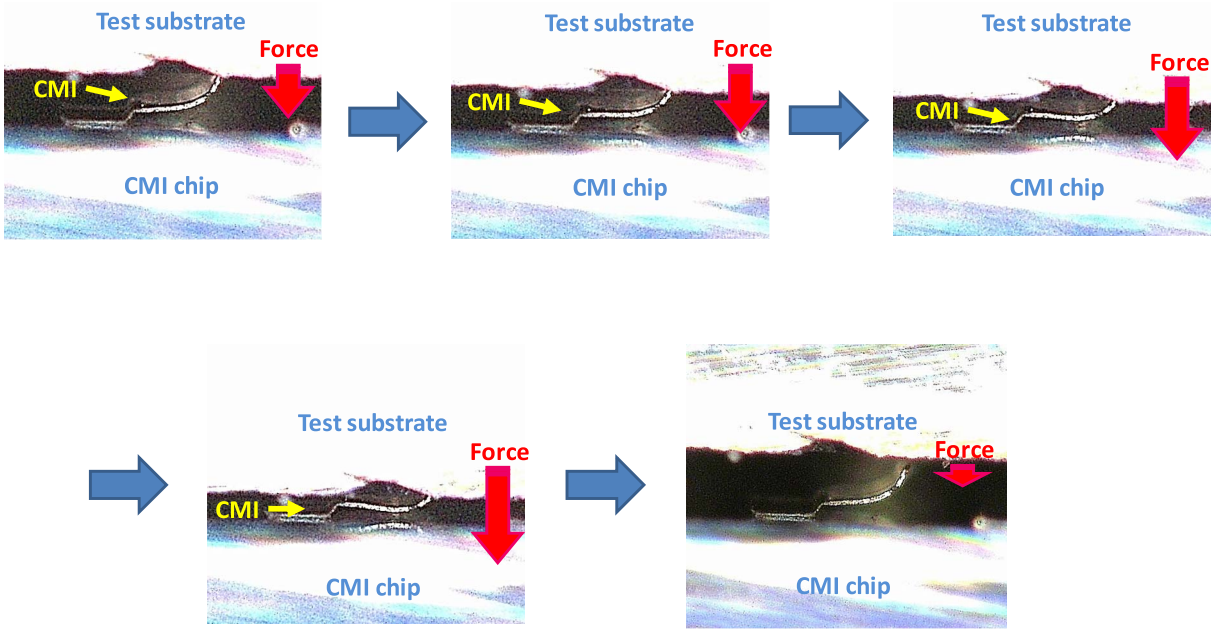


Fig. 9. Cross-sectional view of the assembled chip while applying force from the top substrate. It is shown that CMIs deflect with force.

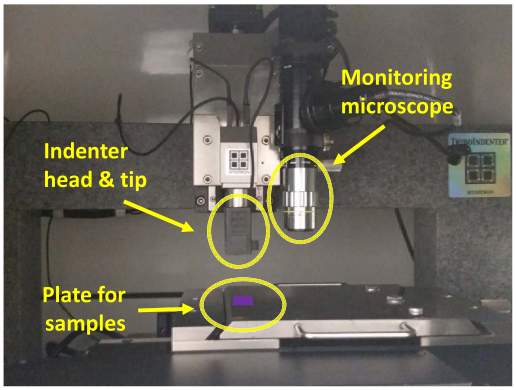
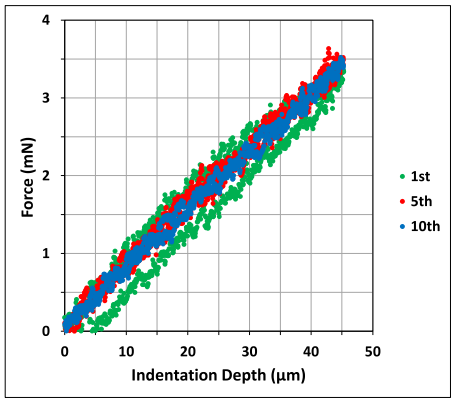


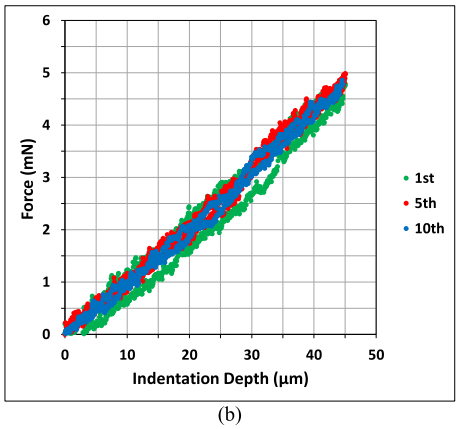
Fig. 10. Compliance measurement using Hysitron Triboindenter.

to hold the chip onto the test substrate, as shown in Fig. 7(c), to facilitate measurements. In order to check the alignment between the CMIs and pads after flip-chip bonding, X-ray imaging was performed using a Dage X-Ray XD7600NT. Fig. 8 shows the X-ray image of the assembled chip, which upon visual inspection reveals an accurate alignment.

In order to investigate the real-time motion of the CMIs during deformation, a cross-section of the assembled chip was recorded before the epoxy was applied using a Keyence VHX-600 Digital Microscope. Fig. 9 shows the motion of the CMI when the applied force increases while the gap between the chip and substrate is decreased. Even after several instances of deformation, the CMI returns to its original position, which is indicative of elastic behavior. This also demonstrates that the CMI maintains electrical contact with the pad via its tip during deflection.



(a)



(b)

Fig. 11. Force versus indentation depth curve of CMI with (a) 7.6 μm thickness and (b) 10.5 μm thickness.

B. Mechanical Characteristics

Compliance, which is the inverse of stiffness, is a key property of flexible interconnects since it is related to the interconnect's ease of vertical motion within the elastic region during the assembly process. Fig. 10 illustrates the measurement setup for CMI compliance using a Hysitron Triboindenter with a cono-spherical probe tip.

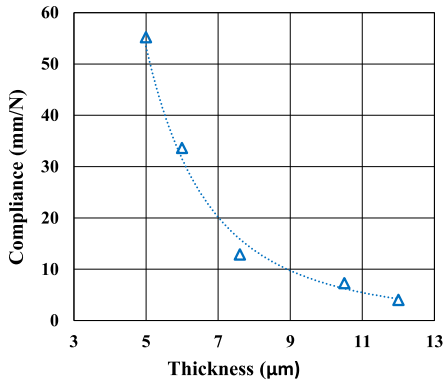


Fig. 12. ANSYS compliance data as a function of thickness.

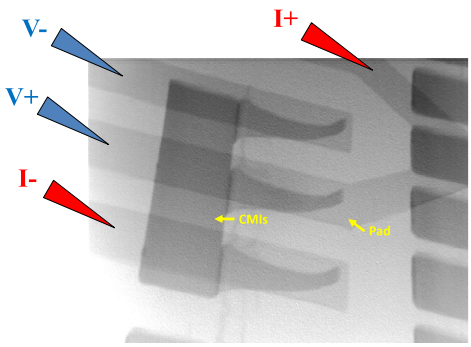


Fig. 13. CMI structure for four-point resistance measurement.

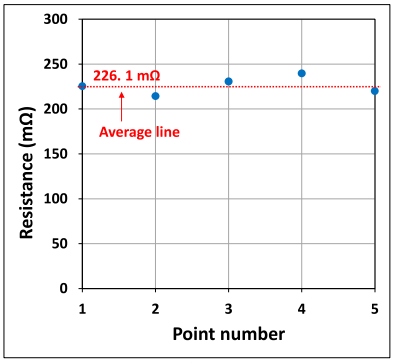
Compliance of the CMI was measured by positioning the cono-spherical probe tip directly on the top flat area of the CMI; this was done for both CMI thickness values of 7.6 and 10.5 μm. In each indentation cycle, there are two steps: a downward moving step and an upward moving step. During the downward motion of indentation, the CMI is deformed downward by the probe tip to a preset depth, and the applied force versus displacement data of the CMI is recorded. In the same way, the reaction force of the CMI on the probe while it recovers to its original position is recorded during the upward motion of indentation. The CMI was deflected downward by 45 μm, and the indentation test was repeated ten times on the same CMI to confirm repeatability.

The results of the indentation tests are shown in Fig. 11. Fig. 11(a) is the force versus indentation depth graph of the 7.6-μm-thick CMI, and Fig. 11(b) is that of the 10.5-μm-thick CMI. As seen in Fig. 11, the initial indentation shows some minor plastic deformation. However, the CMI undergoes elastic recovery, and hence all subsequent indentations attain up to 45 μm of vertical elastic deformation and continue to do so even after several deflection cycles.

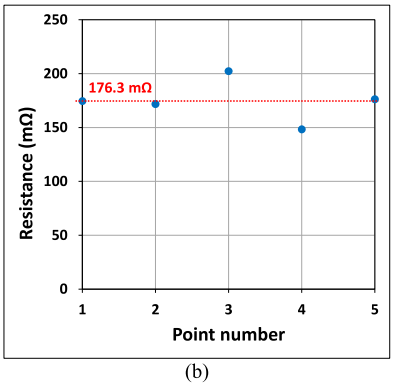
The compliance data from the measurements and simulations are shown in Table III. The compliance of the 7.6- and 10.5-μm-thick CMIs is 13.12 and 9.34 mm/N, respectively. Using ANSYS FEM simulations, similar compliance data was obtained for the tested CMIs. Additional compliance simulation data with other thickness values are shown in Fig. 12; compliance increases significantly as the thickness decreases. Therefore, this allows us to engineer a wide range of compliance values simply by adjusting the thickness of the CMIs; the thickness of CMIs can be modified by adjusting the time of the electroplating process. Thus, a specific compliance can be attained depending on application requirements.

TABLE III
COMPLIANCE DATA FROM SIMULATION AND MEASUREMENT

		Thickness	
		7.6 μm	10.5 μm
Compliance (mm/N)	Simulation	12.9	7.3
	Indentation measurement	13.12	9.34



(a)



(b)

Fig. 14. Four-point resistance of CMIs with (a) 7.6 μm thickness and (b) 10.5 μm thickness.

TABLE IV
RESISTANCE DATA FROM MEASUREMENT

	Thickness	
	7.6 μm	10.5 μm
Average four-point resistance (mΩ)	226.1	176.3

C. Electrical Characteristics

The electrical resistance of the CMIs with a "blunt tip" was measured by performing a four-point resistance measurement with a Signatone probe station. The CMI four-point resistance structure, which consists of three CMIs sharing a single anchor, as shown in Fig. 13, was used to measure the CMI four-point resistance. Since the CMI chip and the test

substrate are flip-chip bonded, CMIs are partially bent, and therefore the tips of the CMIs remain in contact with the corresponding mating pads. By applying a current source and using a voltmeter on the appropriate contact pads, resistance data, which includes the resistance of the CMI and the contact resistance, can be measured. The results are summarized in Fig. 14 and Table IV. The average four-point resistance of the 7.6-μm-thick CMIs is 226.1 mΩ, and that of the 10.5-μm-thick CMIs is 176.3 mΩ.

V. Conclusion

In this paper, highly flexible NiW CMIs are batch fabricated using standard CMOS-compatible processes. The CMIs, with an in-line pitch of 150 μm, demonstrate up to 45 μm vertical range of motion within the elastic region. In addition, the CMIs show favorable mechanical and electrical characteristics; the measured compliance of the fabricated CMIs is as high as 13.12 mm/N, while the four-point resistance, including contact resistance, is as low as 176.3 mΩ. Along with these measured characteristics, the real-time motion of CMIs during bonding demonstrates the compliant and temporary contact between two substrates. Since CMIs are lithographically defined, they can easily keep pace with I/O pad size and pitch reduction. Lastly, the high degree of freedom in interconnect design enables CMIs to be easily engineered, and therefore this can allow CMIs to be used in various applications.

References

[1] M. S. Bakir and J. D. Meindl, *Integrated Interconnect Technologies for 3D Nanoelectronic Systems*. Norwood, MA, USA: Artech House, 2009.

[2] J. D. Meindl, "The evolution of monolithic and polylithic interconnect technology," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, USA, Jun. 2002, pp. 2–5.

[3] R. Mahajan *et al.*, "Embedded multi-die interconnect bridge (EMIB)—A high density, high bandwidth packaging interconnect," in *Proc. IEEE 66th Electron. Compon. Technol. Conf. (ECTC)*, vol. 3. Las Vegas, NV, USA, May/Jun. 2016, pp. 557–565.

[4] M. S. Bakir, B. Dang, R. Emery, G. Vandentop, P. A. Kohl, and J. D. Meindl, "Sea of leads compliant I/O interconnect process integration for the ultimate enabling of chips with low-k interlayer dielectrics," *IEEE Trans. Adv. Packag.*, vol. 28, no. 3, pp. 488–494, Aug. 2005.

[5] M. S. Bakir *et al.*, "Sea of leads (SoL) ultrahigh density wafer-level chip input/output interconnections for gigascale integration (GSI)," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2039–2048, Oct. 2003.

[6] B. Dang, M. S. Bakir, C. S. Patel, H. D. Thacker, and J. D. Meindl, "Sea-of-leads MEMS I/O interconnects for low-k IC packaging," *J. Microelectromech. Syst.*, vol. 15, no. 3, pp. 523–530, Jun. 2006.

[7] K. Kacker, G. C. Lo, and S. K. Sitaraman, "Low-K dielectric compatible wafer-level compliant chip-to-substrate interconnects," *IEEE Trans. Adv. Packag.*, vol. 31, no. 1, pp. 22–32, Feb. 2008.

[8] K. Kacker and S. K. Sitaraman, "Electrical/mechanical modeling, reliability assessment, and fabrication of flexconnects: A MEMS-based compliant chip-to-substrate interconnect," *J. Microelectromech. Syst.*, vol. 18, no. 2, pp. 322–331, Apr. 2009.

[9] Q. Zhu, L. Ma, and S. K. Sitaraman, "β-Helix: A lithography-based compliant off-chip interconnect," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, no. 3, pp. 582–590, Sep. 2003.

[10] S. Muthukumar *et al.*, "High-density compliant die-package interconnects," in *Proc. 56th Electron. Compon. Technol. Conf.*, San Diego, CA, USA, Jun. 2006, p. 6.

[11] H. S. Yang and M. S. Bakir, "Design, fabrication, and characterization of freestanding mechanically flexible interconnects using curved sacrificial layer," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 4, pp. 561–568, Apr. 2012.

[12] C. Zhang, H. S. Yang, and M. S. Bakir, "Highly elastic gold passivated mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1632–1639, Oct. 2013.

[13] C. Zhang, H. S. Yang, and M. S. Bakir, "Mechanically flexible interconnects with highly scalable pitch and large stand-off height for silicon interposer tile and bridge interconnection," in *Proc. IEEE 64th Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, USA, May 2014, pp. 13–19.

[14] I. Shubin *et al.*, "Novel packaging with rematable spring interconnect chips for MCM," in *Proc. 59th Electron. Compon. Technol. Conf. (ECTC)*, San Diego, CA, USA, May 2009, pp. 1053–1058.

[15] L. Ma, Q. Zhu, T. Hantschel, D. K. Fork, and S. K. Sitaraman, "J-springs—Innovative compliant interconnects for next-generation packaging," in *Proc. 52nd Electron. Compon. Technol. Conf. (ECTC)*, San Diego, CA, USA, May 2002, pp. 1359–1365.

[16] R. B. Marcus, "A new coiled microspring contact technology," in *Proc. 51st Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, USA, Jun. 2001, pp. 1227–1232.

[17] S. H. Lee, K. N. Chen, and J. J. Q. Lu, "Wafer-to-wafer alignment for three-dimensional integration: A review," *J. Microelectromech. Syst.*, vol. 20, no. 4, pp. 885–898, Aug. 2011.

[18] M. Zia *et al.*, "3-D integrated electronic microplate platform for low-cost repeatable biosensing applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 12, pp. 1827–1833, Dec. 2016.

[19] Y. Zhao and K. Chakraborty, "Cross-contamination avoidance for droplet routing in digital microfluidic biochips," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 31, no. 6, pp. 817–830, Jun. 2012.

[20] L. Loo *et al.*, "A rapid method to regenerate piezoelectric microcantilever sensors (PEMS)," *Sensors*, vol. 11, no. 5, pp. 5520–5528, May 2011.

[21] E. Slavcheva, W. Mokwa, and U. Schnakenberg, "Electrodeposition and properties of NiW films for MEMS application," *Electrochim. Acta.*, vol. 50, no. 28, pp. 5573–5580, Sep. 2005.

[22] M. B. Renee and C. W. Robert, "Fiber pullout behavior and impact toughness of short shaped copper fibers in thermoset matrices," *Compos. A, Appl. Sci. Manuf.*, vol. 36, no. 5, pp. 683–690, May 2005.

Paul K. Jo (S'15) received the B.S. (Highest Hons.) and M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2009 and 2011, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with the Georgia Institute of Technology, Atlanta, GA, USA.

His current research interests include 2.5-D/3-D heterogeneous integration and biosensor application using novel microfabricated flexible interconnect technologies.

Muneeb Zia (S'14) received the B.S. (Highest Hons.) degree in electronic engineering from the Ghulam Ishaq Khan Institute of Science and Technology, Topi, Pakistan, in 2010, and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2013.

His current research interests include the fabrication and characterization of flexible interconnects and packaging for silicon photonics and bio-sensing platforms.

Joe L. Gonzalez (S'15) received the B.S. (Highest Hons.) and M.S. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2012 and 2014, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interests include improving the mechanical and electrical characteristics of compliant off-chip interconnect for 2.5-D/3-D IC systems.

Hanju Oh (S'14) received the B.S. degree in electrical and computer engineering from Hanyang University, Seoul, South Korea, in 2010, and the M.S. degree from the Georgia Institute of Technology, Atlanta, GA, USA, in 2014, where he is currently pursuing the Ph.D. degree in electrical and computer engineering.

Mr. Oh was a recipient of the Best Student Paper Award of the IEEE Global Interposer Technology Workshop in 2014 and a co-recipient of the Best Poster Award in the thermal track at the Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems in 2014. He received the 2015 Charles Hutchins Educational Grant Award from the Surface Mount Technology Association and the Circuits Assembly Magazine.

Muhannad S. Bakir (S'98–M'03–SM'12) received the B.E.E. degree from Auburn University, Auburn, AL, USA, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 2000 and 2003, respectively.

He is currently a Professor with the School of Electrical and Computer Engineering, Georgia Tech. His current research interests include 3-D electronic system integration, advanced cooling and power delivery for 3-D systems, biosensors and their integration with CMOS circuitry, and nanofabrication technology.

Dr. Bakir was a recipient of the 2013 Intel Early Career Faculty Honor Award, the 2012 DARPA Young Faculty Award, the 2011 IEEE CPMT Society Outstanding Young Engineer Award, and was an Invited Participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium. He and his research group received more than 20 conference and student paper awards, including six from the IEEE Electronic Components and Technology Conference, four from the IEEE International Interconnect Technology Conference, and one from the IEEE Custom Integrated Circuits Conference. His group was awarded the 2014 Best Paper of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY in the area of advanced packaging. He is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES and an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY. In 2015, he was elected by the IEEE CPMT Society to serve as a Distinguished Lecturer.